Delay Line Manchester Decoder

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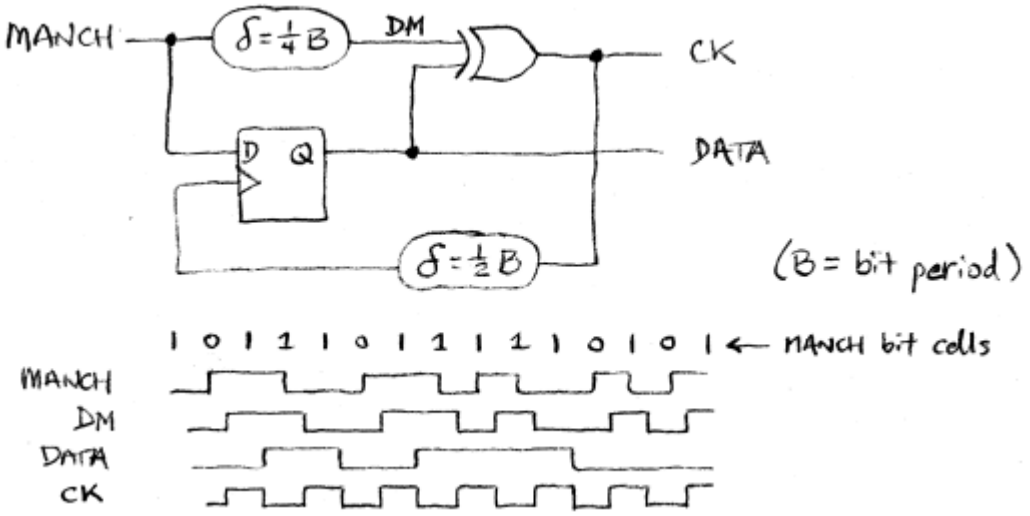

Manchester data encoding is a self-clocked RZ (Return to Zero) form of serial data transmission. It is characterized by a rising edge in the middle of the bit for a '0' and a falling edge for a '1' (see MANCH waveform above). The maximum switching rate of the signal is equal to the bit rate. This occurs when sending a continuous stream of 0s or 1s.

There are various ways of implementing Manchester encoding and decoding, but using two fixed delays, a flip flop, and an EXOR gate as shown here is one of the simplest.

- Note that all CK rising edges are caused by transitions on DM rather than DATA – otherwise the circuit couldn't work.
- There are no race conditions on CK – input edges are always ½ bit apart. Therefore CK edges are always clean.
- Functional analysis: first assume that DATA samples MANCH at the ¼ bit point as shown. Then it is easy to see how CK is generated, and fed-back delayed CK will clock DATA as required.
- Error recovery: errors or powerup can cause DATA to toggle to the wrong state, which will cause CK to invert. Inverted DATA will then persist until a 1-0 or 0-1 data sequence appears on DM. (This is because an inverted CK rising edge comes from DM on repeated bits 1-1 or 0-0 and from DATA on a 1-0 or 0-1 bit change, but DATA won't toggle because it's not sampling the first half-bit of MANCH properly.) There may be an extra or missing CK pulse during the error and recovery period.